APPLICATION NOTE

MP1630B/MP1632C

Digital Data Analyzer

MEASUREMENT SOLUTIONS

ANRITSU CORPORATION

Anritsu

Application Note

Digital Data Analyzer

MP1630B/MP1632C

10 KHz to 200 MHz(MP1630B)

Plug in units

MU163000A 200M Clock Generator Unit
MU163020B 200M 16CH Pulse Pattern Generator Unit
MU163040B 200M 16CH Error Detector Unit

Options

MP1630B-01 GP-IB (for MP1630B)
MP1630B-02 Ethernet (for MP1630B)
MU163000A-01 Jitter Addition (for MU163000A)

50 MHz to 3200 MHz(MP1632C)

Plug in units

MU163220C 3.2G Pulse Generator Unit
MU163240C 3.2G Error Detector Unit

Options

MP1632C-01 GP-IB (for MP1632C)
MP1632C-02 Ethernet (for MP1632C)
MP1632C-03 3.2G Built-in Synthesizer

General purpose error rate measurement instrument which enables eye diagram measurement

MEASUREMENT SOLUTIONS

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Contents

1. Overview

Recently, research and development has progressed in various fields related to optical subscriber systems (e.g., PDS, π system) using burst signal transmission, digital mobile communication (especially W-CDMA), Gigabit Ethernet, fiber channels, and digital broadcasting systems. The demand for measuring instruments to commercialize the results of such research and development has thus been increasing.

The MB1630B can be used to evaluate digital ICs for communication and general-use purposes using its 16-channel simultaneous measurement and mix pattern measurement functions.

2. Application

The MP1630B can evaluate various application devices and can improve productivity through 16-channel simultaneous measurement.

PDS measurements are being simplified by the private screen provided.
This section describes the measurement method for various application.

2.1 PDS (Low-speed PDS/π system)

Frequency: 49.195 MHz

2.1.1 PDS Measurement

Fig.1 shows the configuration of PDS.

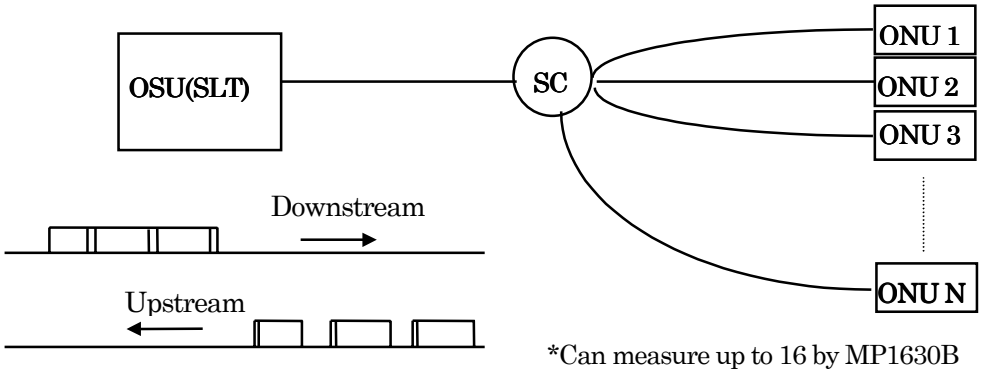
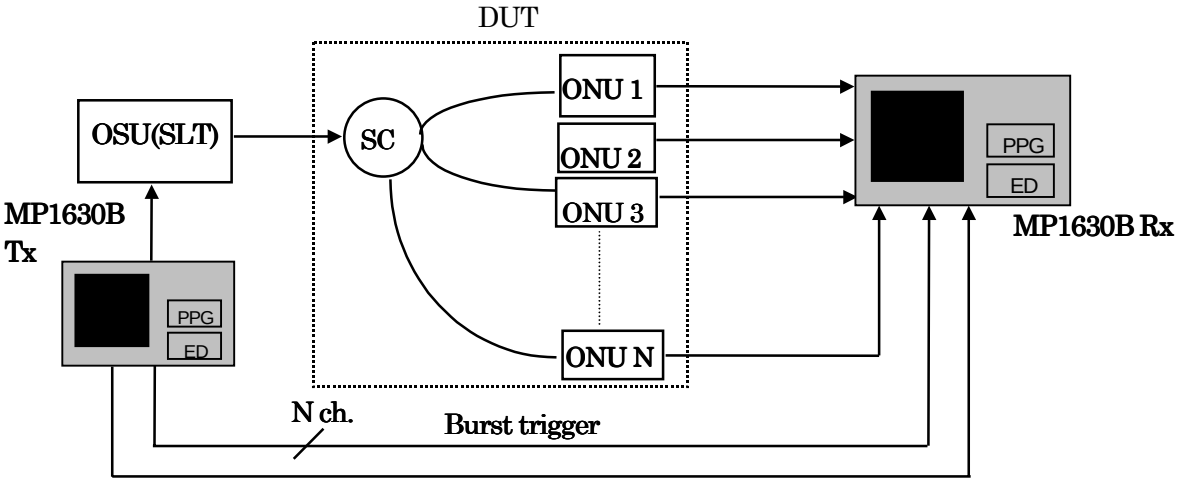


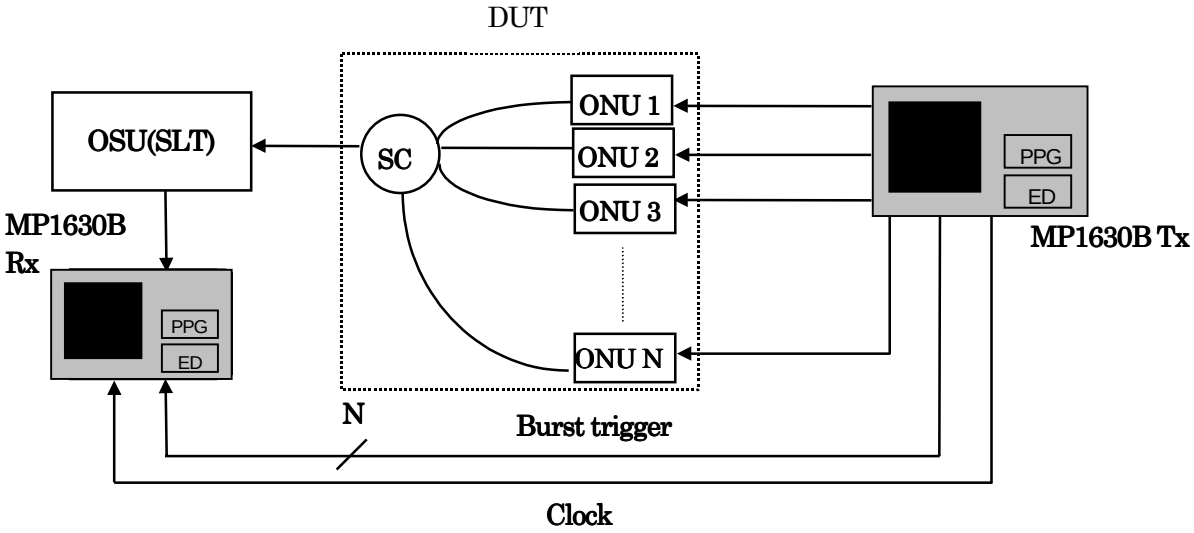
Fig.1

1) Measurement of downstream signal



OSU : Optical subscriber unit
ONU : Optical network unit
SLT : Subscriber line terminal
SC : Star coupler

2) Measurement of upstream signal

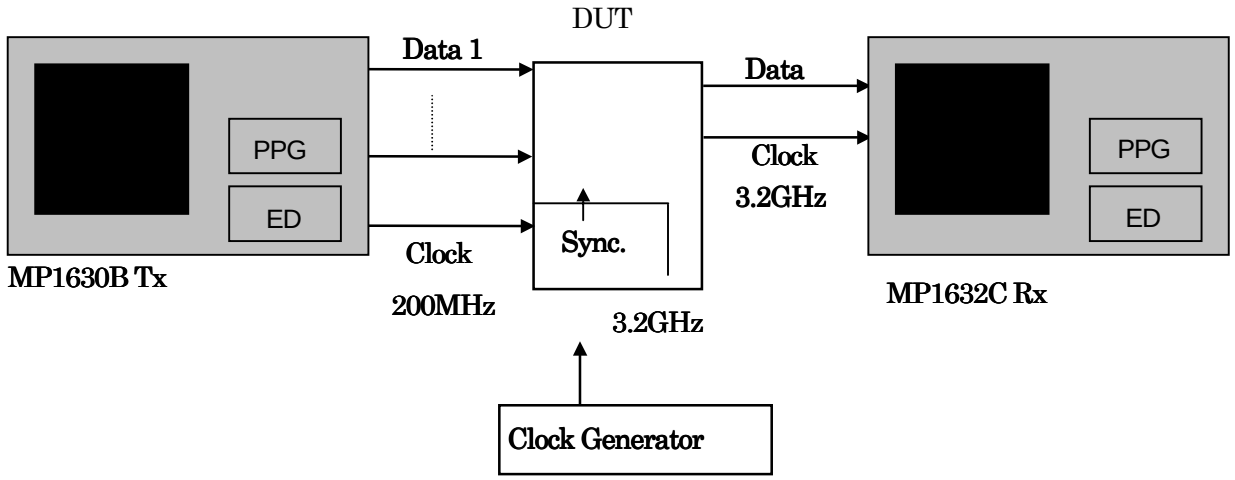


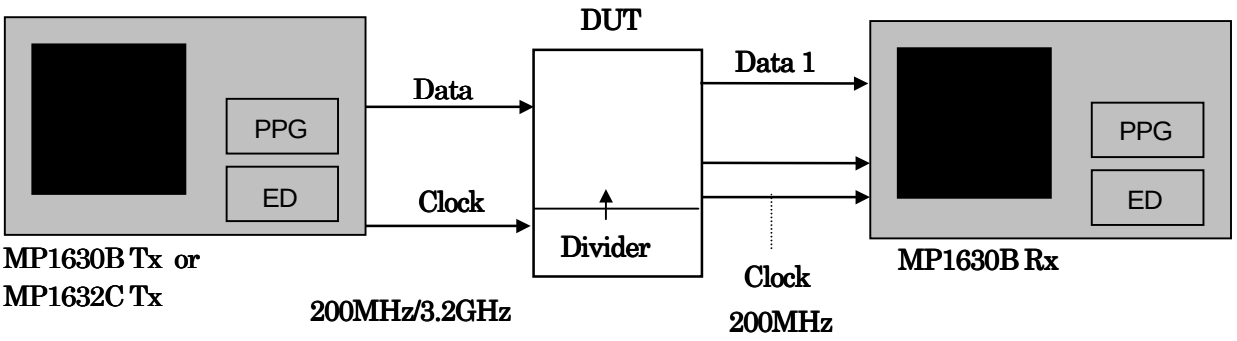
2.2 ATM-PDS (High-speed PDS)

Frequency: Upstream 155.52 MHz
Downstream 155.52 MHz/622.08 MHz

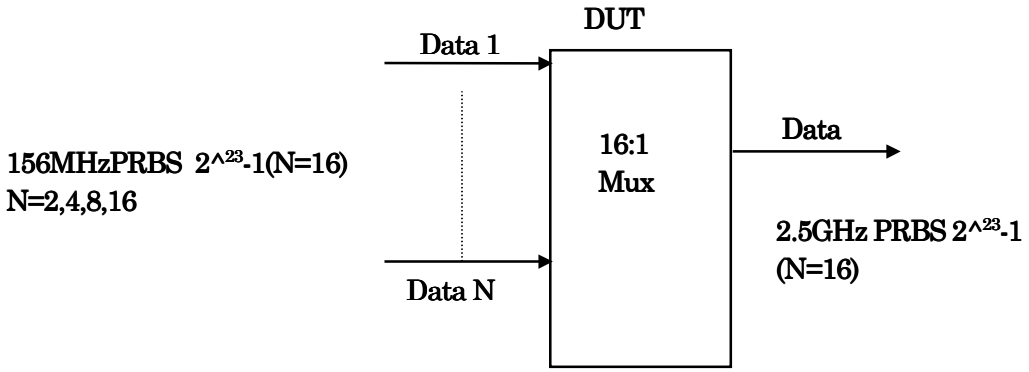
The measurement method is the same as that for 49.152 MHz.
Note that the MP1630B is not applicable with 622.08 MHz.

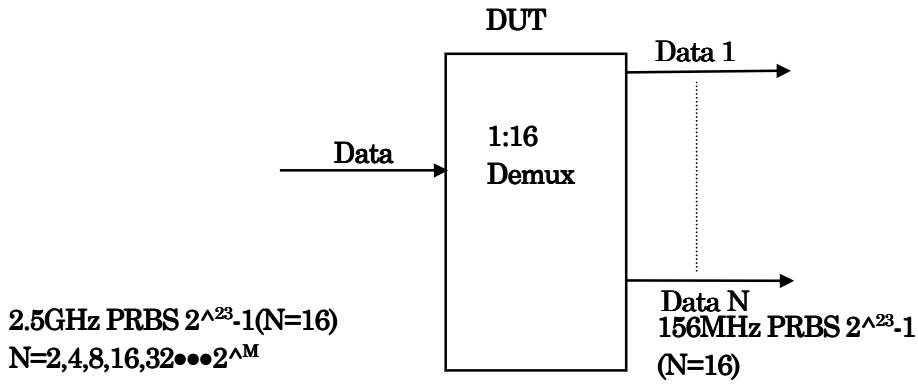
2.3 Multiplexer/Demultiplexer



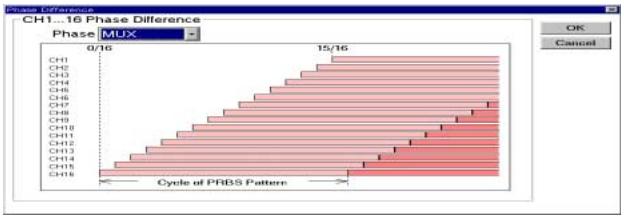


<Note>

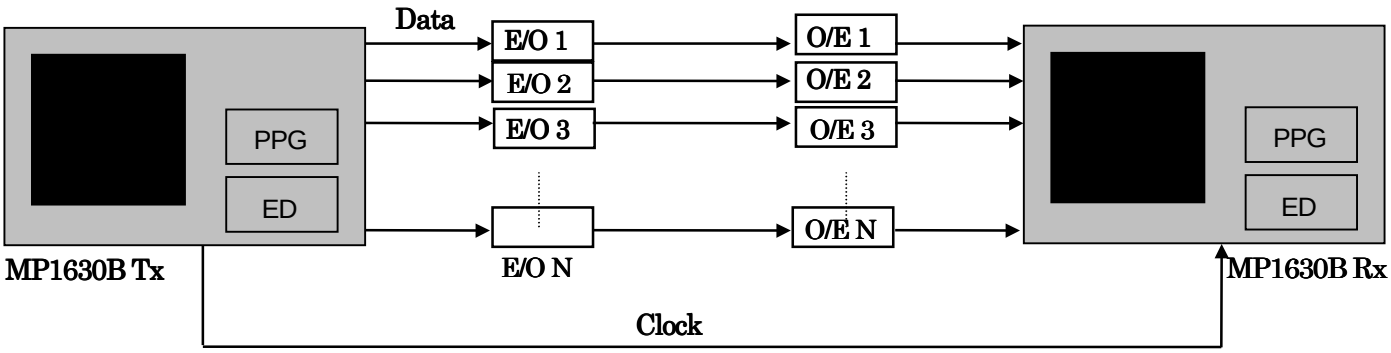




In measurement construction above, the input pattern (e.g. PRBS23) is output as it is.
This is one of Anritsu BERTS features and it enables BER measurement by normal PRBS.



2.4 Optical Device (Parallel measurement)



2.5 Device for Ethernet

< Background>

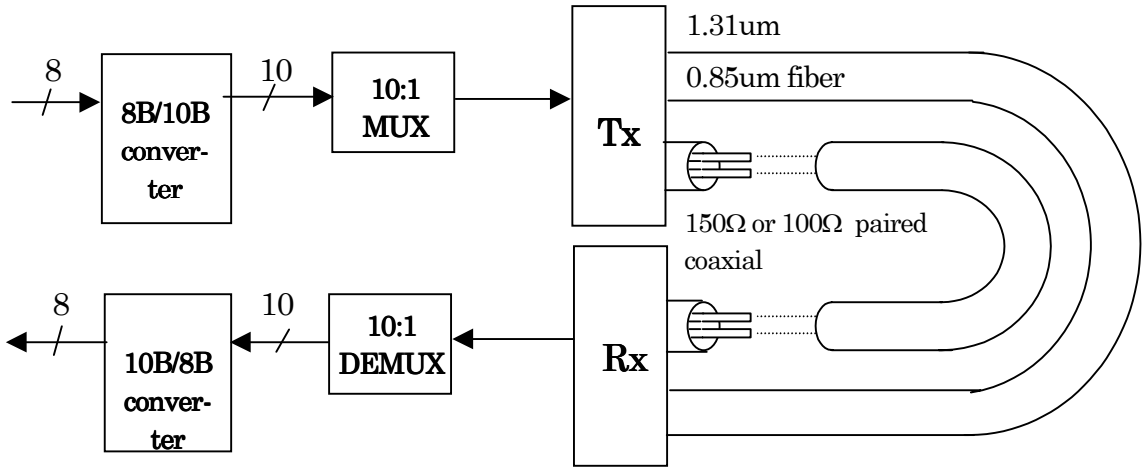
- Enabling large-capacity LAN and WAN backbone networks
- 10 Mb/s→100 Mb/s→1.25 Gb/s→10 Gb/s
- Establishing 1000BASE-T standard (IEEE802.3) compatible with 10BASE-T(10Mb/s) and 100BASE-T(100Mb/s)
- Enabling adoption of 8b/10b code conversion used in the prior technology for fiber channel
- Enabling seamless transmission and network equipment

<Specification>

1)1000 BASE-X (IEEE802.3Z) Encode:8B/10B
1000BASE-LX (1.3um Fiber)
1000BASE-SX (0.85um Fiber)
1000BASE-CX (Paired coaxial cable with shield)

2)1000BASE-T (IEEE802.3ab) ———— CTP twisted cable without shield

<Circuit configuration>



<Application of digital data analyzer>

- Evaluation of CX-compatible paired coaxial cable (150Ω, 100Ω)

  Evaluating cable characteristics using eye-opening of BER.

- Evaluation of SX- and LX-compatible optical module (E/O, O/E)

  BER and eye margin tests using the jitter test pattern specified in the IEEE 802.3

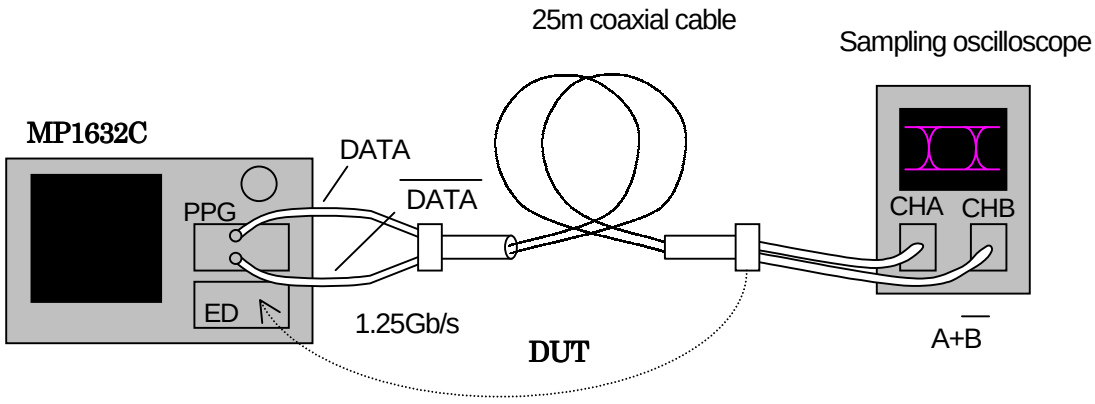
- IC margin test at 1.25 Gb/s

  10:1 MUX/DEMUX, 8b/10b converter, laser driver/receiver,

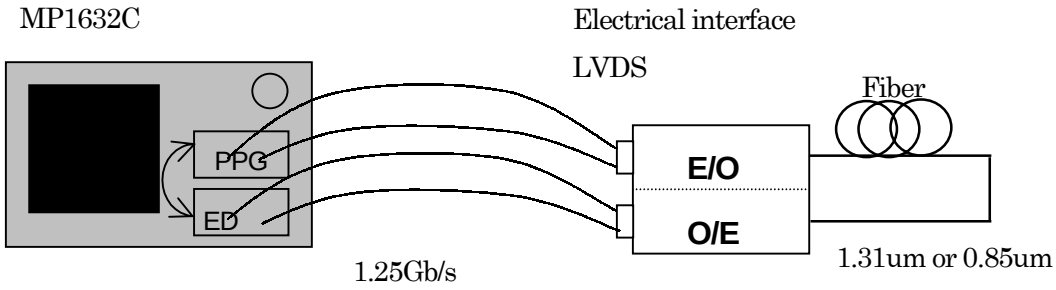
  BER test using a jitter test pattern

<Application example>

1) BER and balance evaluation of balanced cable with shield

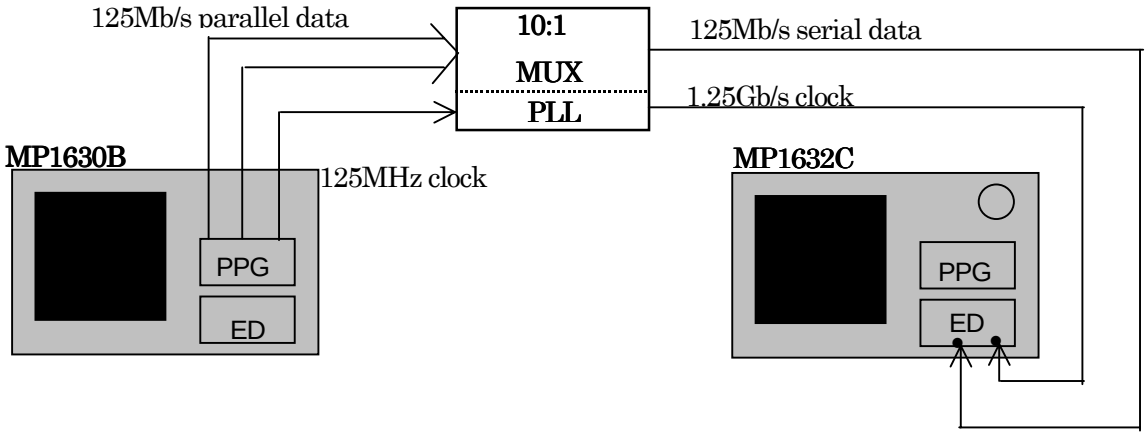


2) E/O, O/E module measurement example



- BER measurement
- Eye margin measurement (E0.0x10^{-12})

3 Evaluation of the functions of the 10:1 multuplexer IC



- 16 ch data generation
- IEEE jitter pattern

- BER measurement
- Eye margin measurement (E0.0x10^{-12})

<Jitter test pattern of IEEE 802.3 standard>

- High frequency bandwidth test pattern

101010……..Eye margin measurement at BER=10^{-12} in continuous pattern

(Random jitter measurement)

- Low frequency bandwidth test pattern

1111100000…….Eye margin measurement and PLL operation test in continuous pattern

• Mixed frequency bandwidth test pattern

Eye margin test (RJ and DJ measurement) in FAC14FAC14 (H) repeated pattern

(RJ : Random Jitter , DJ: Deterministic Jitter)

<10Gb/s Ethernet standardization trends>

Source: IEEE802.3 Higher Speed Study Group

• Starting standardization of 10Gb/s Ethernet in March 1999

• Leading providers/manufacturers

IBM, Texas Instrument, Vitesse, 3COM, Intel, Finisar,

Lucent, Sun Microsystems, MCI Worldcom, HP, Nortel, CANARI

• Operation bit rate 12.4Gb/s

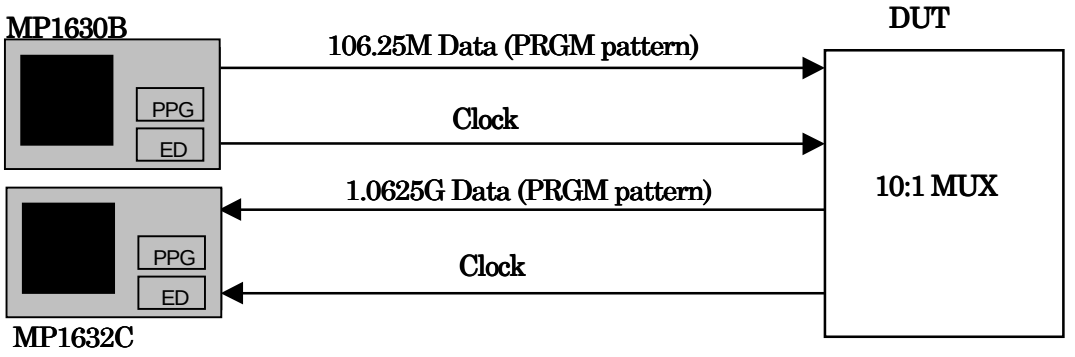
(Anritsu has 12.5Gb/s BERTS for development of 10Gb/s Ethernet.)

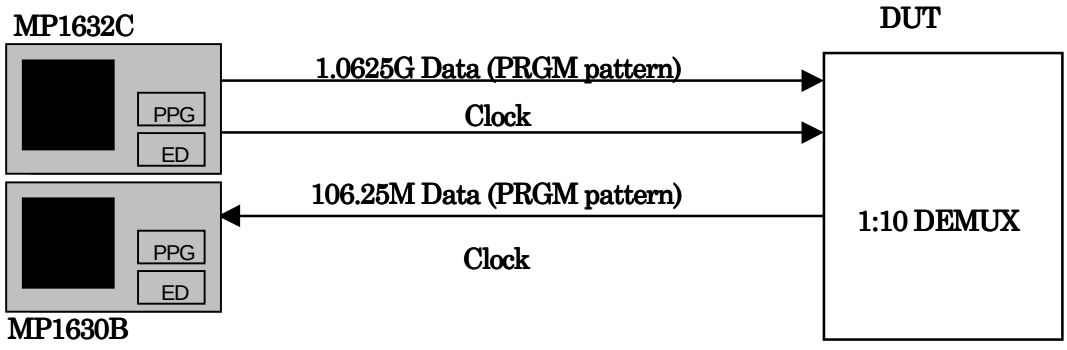
2.6 Device for Fiber Channel

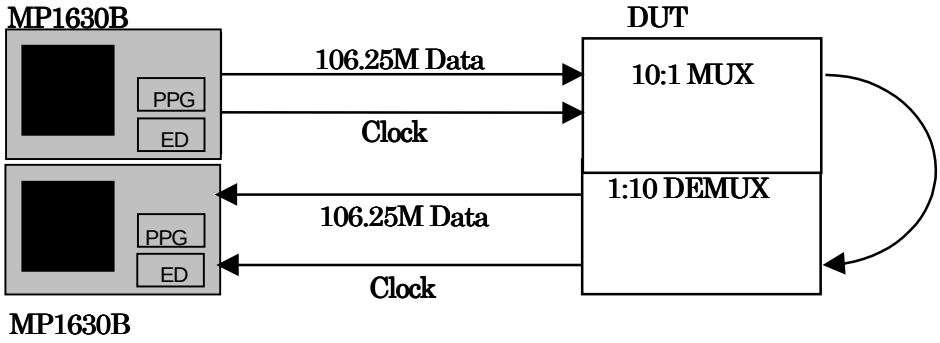
Frequency : 265.6 MHz/531.25 MHz/1,062.5 MHz

Can evaluate key devices used for fiber channel.

1) 10:1 MUX & 1:10 DEMUX testing

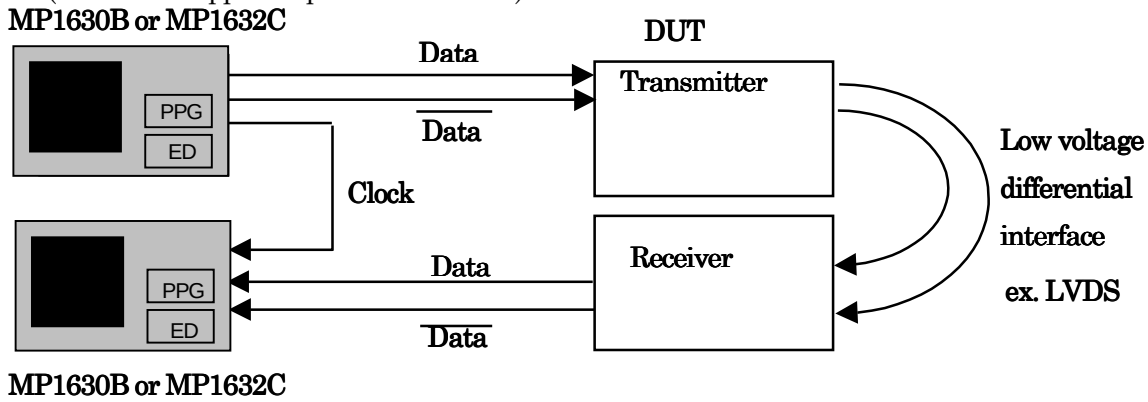






2.7 Device for IEEE1394

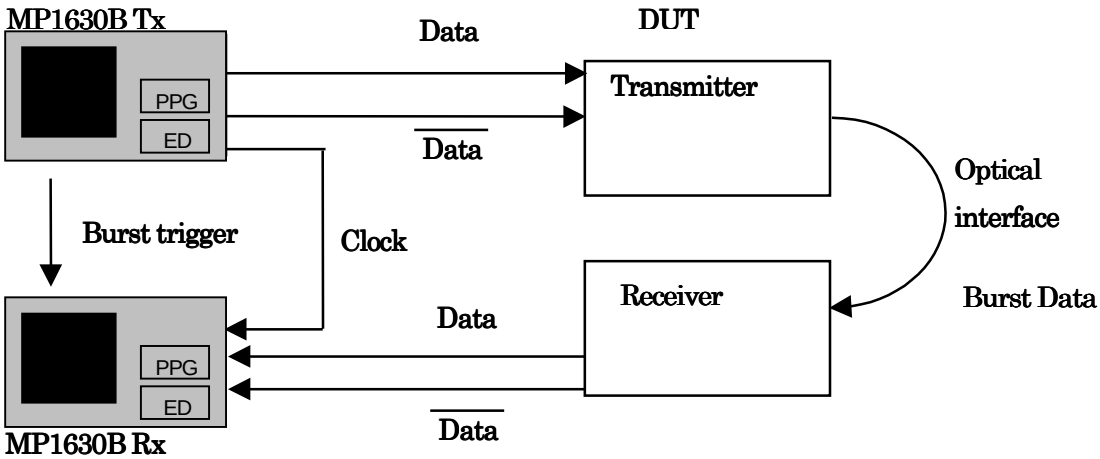
Frequencies: 98.304 MHz, 196.610 MHz, and 393.220 MHz
(MP1630B supports up to 196.610 MHz)



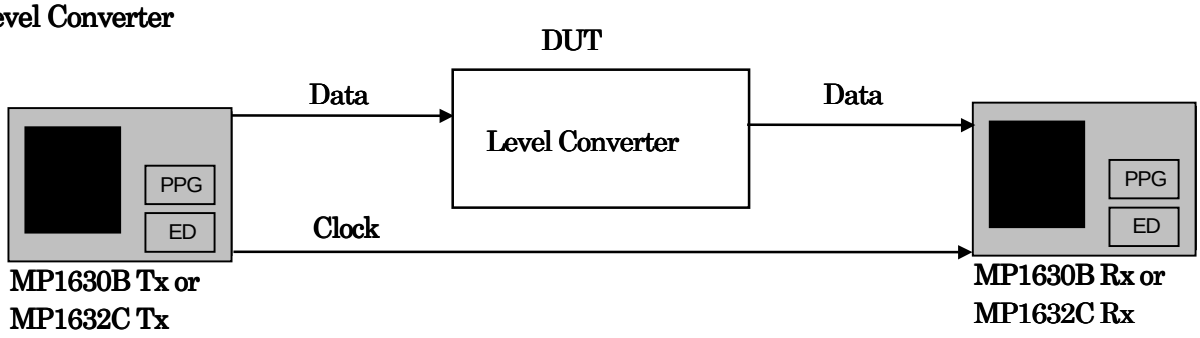
*LVDS Low Voltage Differential Signaling

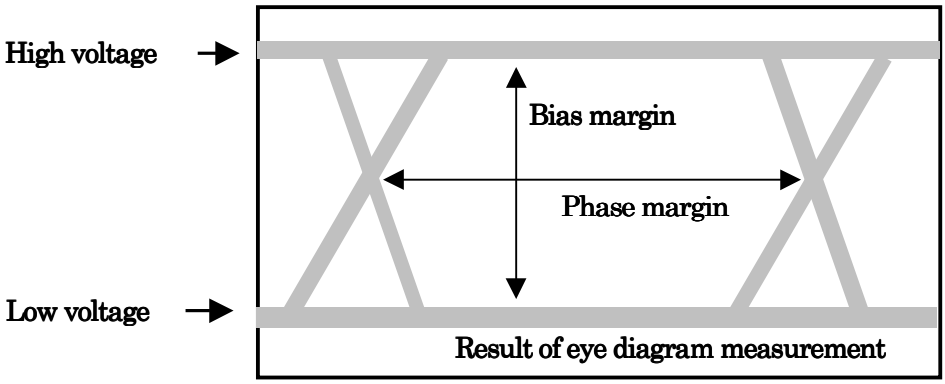
2.8 Device for CATV

Frequencies : up to 50 MHz



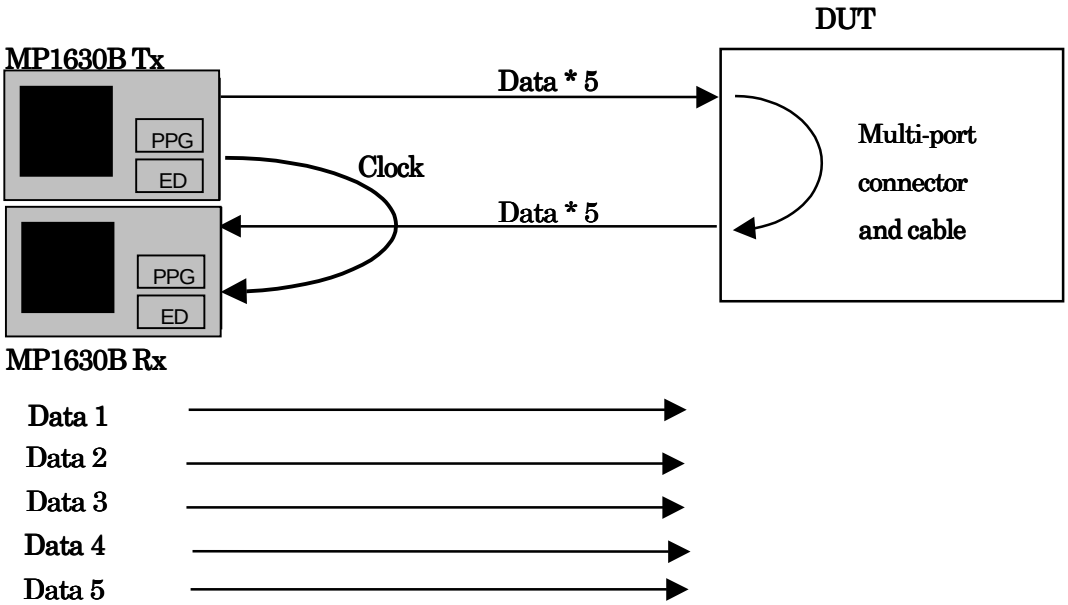
2.9 Level Converter



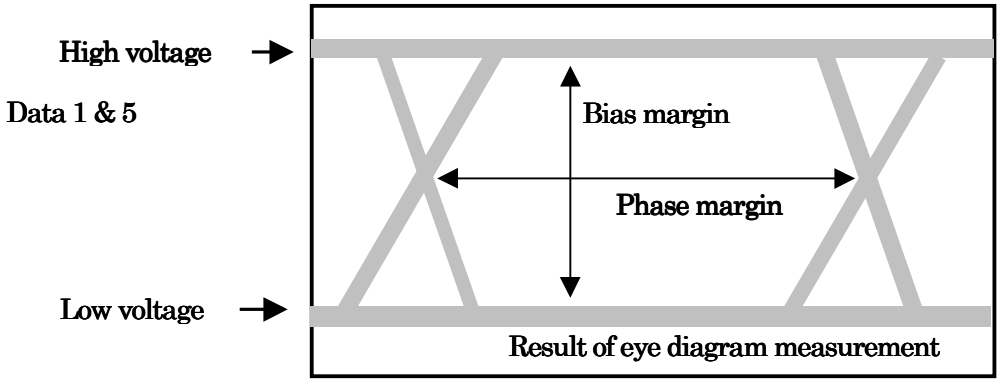


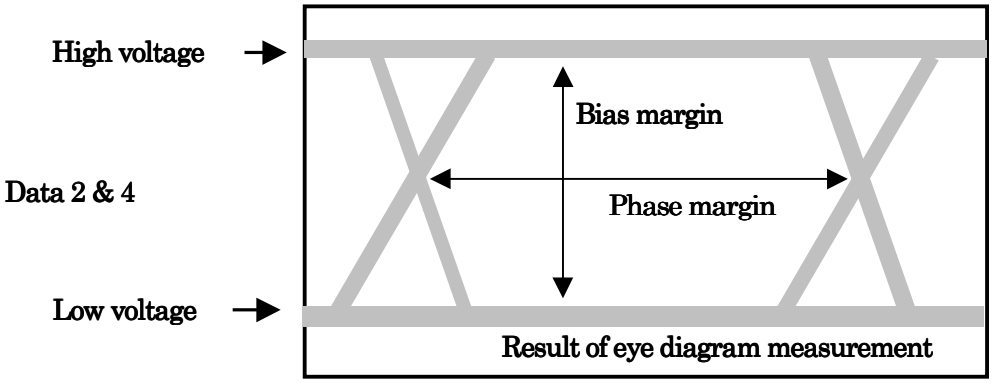
2.10 Evaluation of Multi-port Connector (Cable)

The MP1630B can evaluate effects on adjacent signal lines using the error and eye diagram measurements.



Enter a large amplitude signal to Data3 and measure an eye diagram of each channel.
Note that no signal should be entered to non-measured channels.

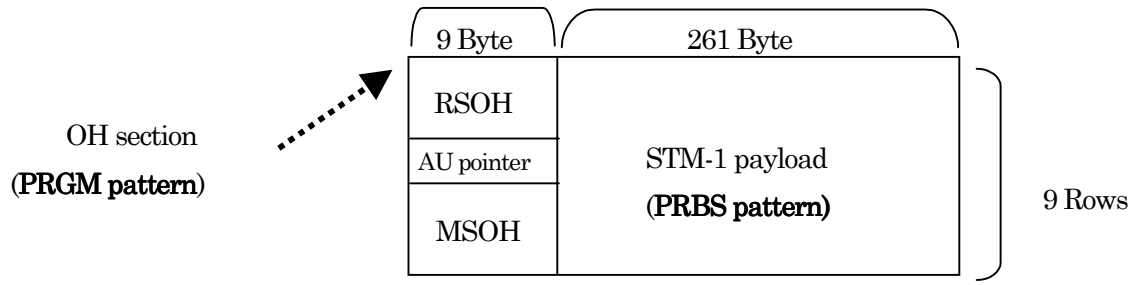


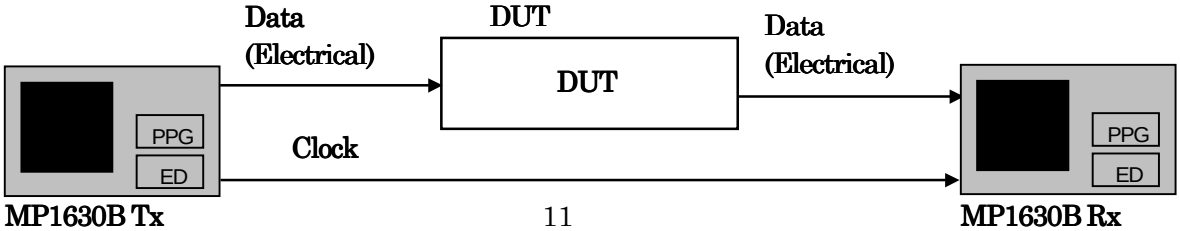


2.11 Evaluation of SDH/SONET Module

A measurement example with a pattern of the SDH/SONET multiplexity configuration frame structure is shown below.

The MP1630B has the MIX pattern function (PRGM／PRBS). Therefore, the following frame configuration can easily be set.





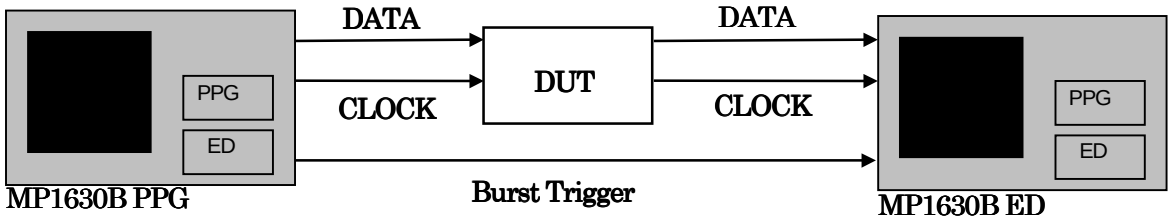
3. Construction of Burst Measurement

This section describes how the MP1630 performs Burst measurement.

Burst measurements are roughly grouped into the following four methods. Besides these methods, Burst measurements can also be performed using a PRGM pattern and MIX pattern.

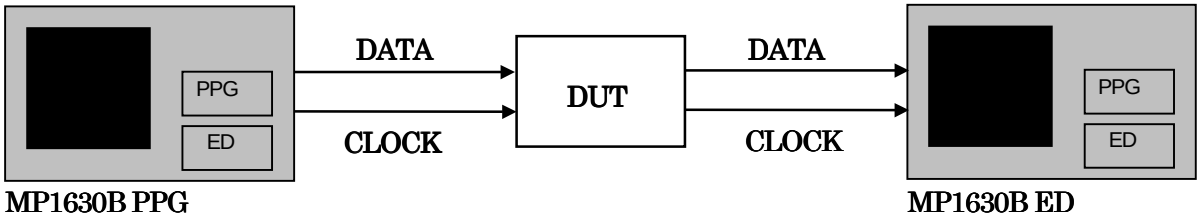
1) Method using burst trigger (Burst Sync Mode: EXT)

This method performs measurement by sending a signal (Burst Trig.) which indicates the enable region (part containing data) in the Burst signal from the PPG. Measurement can be performed without dropping a single bit, but only the near end is measured because PPG and ED must be directly connected.



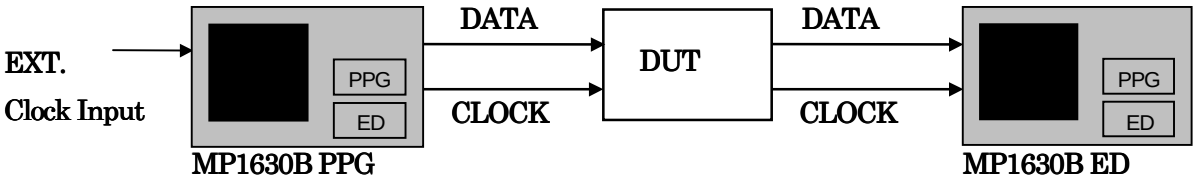
2) Method using frame synchronization (Burst Sync Mode: INT)

A special pattern is inserted at the head of the burst signal, and ED measurement is performed by making this special pattern the start point. Measurement is performed at the near end because PPG and ED must be directly connected. However, if there is a special pattern at other than the head of the burst signal, ED measurement causes non-synchronization and may be impossible to perform.



3) Method which supplies an external Burst Clock (Using EXT Clock Input)

The Burst signal is generated by inputting an external Burst Clock. Since the measuring instrument can be used in the Normal state, measurement is possible even with the conventional type BERTS. Since the logic of the preceding data determines the level of the data Disable region (part where there is no data), it changes depending on whether this logic is high or low.



4) How to edit burst data using a pattern

This method generates Burst data with part of the PRGM or MIX pattern at the "0" ("low") level. The disable zone also becomes the error measurement region. If multiple errors are generated in the disable zone, the instrument might not shift to the synchronous state.

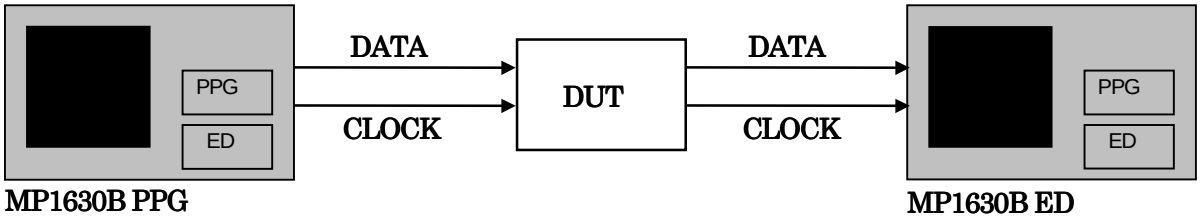


Table 1 shows the settings of the above four methods.

Table 1

	Clock source	Tx mode	Rx mode	Burst Cycle	connection	Other
1)	INT/EXT	Burst	Burst	INT/EXT	Data/Clock/Burst Trig.	
2)	INT/EXT	Burst	Burst	INT/EXT	Data/Clock	
3)	EXT	Normal	Normal	depend on clock	Data/Clock	
4)	INT/EXT	Normal	Normal	pattern length	Data/Clock	

3.1 Setting Method

3.1.1 Input/Output Phase

The PPG output phase and optimum ED input phase are shown below. These phases are necessary to make the ideal phase conditions for both Normal and Burst.

1) PPG output phase

PPG has five output signals: Clock, Data, Sync. Trigger, Burst Trigger, and AUX. Figure 3.1.1 shows the phase relationships between these signals. The Data and Clock output phase settings are both 0 ns, and the Burst Trigger bit phase is 0 bit.

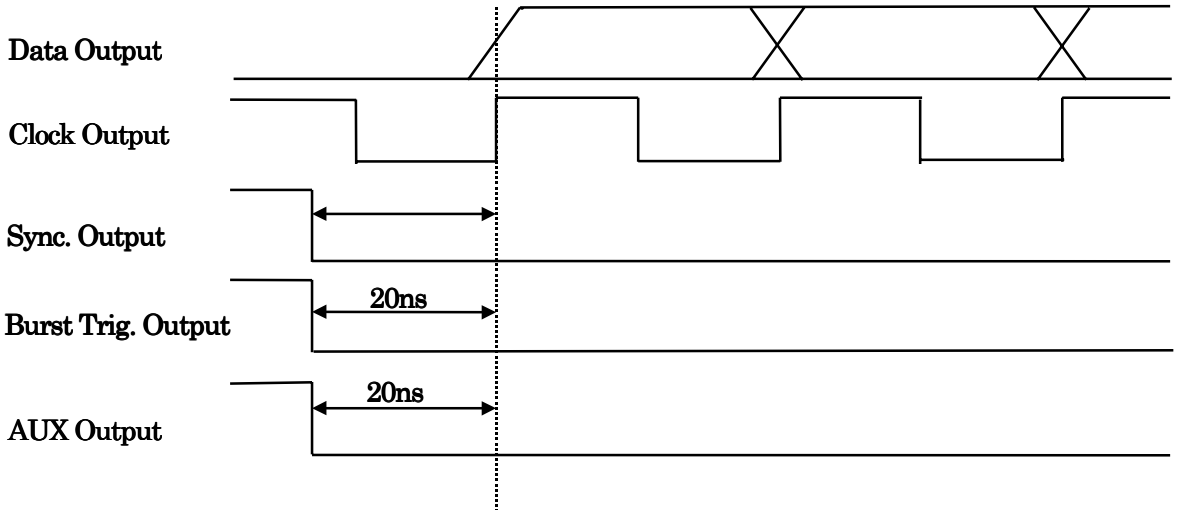


Fig. 3.1.1

2) ED input phase

ED has three input signals: Clock, Data, and Burst Trigger. Figure 3.1.2 shows the optimum phase relationships between these signals. The Clock input phase setting is 0 ns.

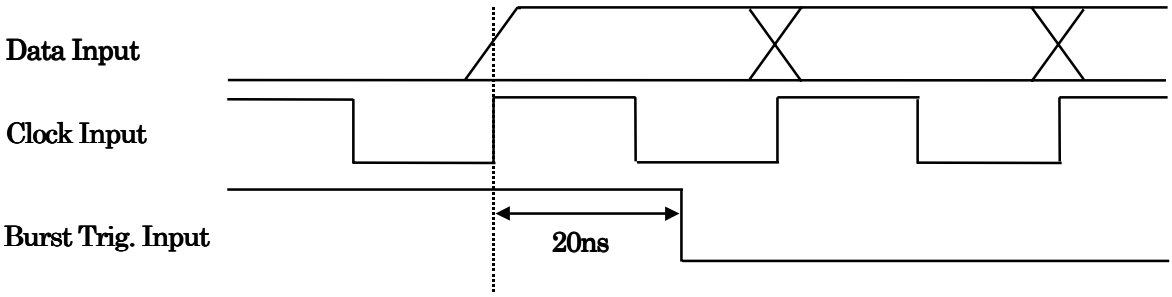


Fig. 3.1.2

The transmitter advances the Burst Trigger 20 ns relative to the Data and Clock signals. Since these signals should be delayed by 20 ns and input at the receiver, an overall delay of 40 ns is necessary. To set the delay in bits, the Burst Trigger requires delay adjustment according to the frequency as follows:

$$\frac{(40 \pm \text{measuring system delay})}{(\text{signal period})} \qquad \text{Units: ns}$$

3.1.2 Measurement Preparations

To perform an error measurement, the input phase must be adjusted and synchronization must be established. If the input to ED has the phase relationship shown in Fig. 3.1.2, ED is the optimum phase. However, the phase can be adjusted without checking with an oscilloscope, etc. by using the procedure below. Depending on the circumstances, adjustment can be performed easier by checking the phase with an oscilloscope.

1) Measuring a system with continuous data

Perform Auto Search by Normal PRBS.

↓

Change to Burst measurement pattern.

↓

(When frame synchronization is used, should be Error Free here.)

↓

Increase the delay in 1-bit increments, starting from the delay obtained from the expression minus 1 bit.

↓

Change the ED side Clock phase, and check the phase margin at the Error Free point.

If the phase margin cannot be obtained, change the PPG side Data and Clock phases by the same amount and search for the point where the phase margin can be obtained.

* If the margin decreases when the ED side Clock is shifted to the minus side, change the PPG side Data and Clock signals to the plus side. If the margin decreases when the ED Clock signal is shifted to the plus side, change the PPG side Data and Clock signals to the minus side.

2) Measuring a system without continuous data

Measure the Burst measurement pattern.
↓
Set all PPG and ED phases to 0 ns.
↓
Increase the delay in 1-bit increments, starting from the delay obtained from the expression - 1 bit.
↓
If not Error Free, reverse the polarity of the ED side clock and repeat from the beginning. Change the ED side Clock phase at the Error Free point, and check the phase margin.
↓
If the phase margin cannot be obtained, change the PPG side Data and Clock phases by the same amount and search for the point where the phase margin can be obtained.

* If the margin decreases when the ED side Clock is shifted to the minus side, change the PPG side Data and Clock to the plus side. If the margin decreases when the ED side Clock is shifted to the plus side, change the PPG side Data and Clock to the minus side.

4. Appendix

Reference: IC evaluation test interface on the use of the MP1630B

1) PPG side

Clock/data output level

	ECL	(V oh: -0.9 V, V ol: -1.7 V)
	PECL	(V oh: +4.0 V, V ol: +3.3 V)
	TTL	(V oh: +5.0 V, V ol: +0.0 V)
	LVTTL	(V oh: +3.3 V, V ol: +0.0 V)
	VER	(for High impedance)
		V oh: -4.500 to +5.000 V/5mV steps
		V ol: -5.000 to +4.500 V/5mV steps
		+0.500V≤V oh-V ol≤+5.000 V/10mV steps
		<50Ω to GND terminating>
		V oh: -2.250 to +2.500 V/2.5 mV steps
		V ol: -2.250 to +2.250 V/2.5 mV steps
		+0.250V≤V oh-V ol≤+2.500 V/5 mV steps
Clock/data terminating conditions	ECL	50Ω to –2 V
	PECL	50Ω to +3 V
	TTL	High impedance
	LVTTL	High impedance
	VER	50Ω to GND/50 Ω to –2 V/50Ω to +3 V and High impedance

2) ED side

Clock input level	V ih : -4.500 to +5.000 V
	V il: -5.000 to +4.500 V
	Vp-p: +0.500 to +5.000 Vp-p
Input terminating condition	50Ω to GND/50Ω to –2 V/50Ω to +3 V
Data input level	V ih: -4.500 to +5.000 V
	V il: -5.000 to +4.500 V
	Vp-p: +0.500 to +5.000 Vp-p
Threshold level (Vth)	: -5.000 to +5.000 V/5 mV steps (at VER GND terminating)
	: -2.000 to -0.600 V/5 mV steps (at VER –2V terminating)
	: +3.000 to +4.400V/5mV steps (at VER +3 terminating)

Input terminating condition	ECL	50Ω to –2 V (Threshold: -1.3V)
	PECL	50Ω to +3 V (Threshold: +3.7V)
	TTL	50Ω to GND (Threshold: +1.4V)
	CMOS	50Ω to GND (Threshold: +2.5V)
	LVTTL	50Ω to GND (Threshold: +1.4 V)
	VER	50Ω to GND/50to –2 V/50 to +3 V

Anritsu

Specifications are subject to change without notice.

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